

DATA SHEET

74ALVT16600

**2.5V/3.3V 18-bit universal bus
transceiver (3-State)**

Product specification
Replaces data of 1997 May 12
IC23 Data Handbook

1998 Feb 13

2.5V/3.3V 18-bit universal bus transceiver (3-State)

74ALVT16600

FEATURES

- 18-bit bidirectional bus interface
- 5V I/O Compatible
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Negative edge-triggered clock inputs
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ALVT16600 is a high-performance BiCMOS product designed for V_{CC} operation at 2.5V and 3.3V with I/O compatibility up to 5V.

This device is an 18-bit universal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. Data flow in each direction is controlled by output enable (\overline{OEAB} and \overline{OEBA}), latch enable (LEAB and LEBA), and clock (\overline{CPAB} and \overline{CPBA}) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is High. When LEAB is Low, the A data is latched if \overline{CPAB} is held at a High or Low logic level. If LEAB is Low, the A-bus data is stored in the latch/flip-flop on the High-to-Low transition of \overline{CPAB} . When \overline{OEAB} is Low, the outputs are active. When \overline{OEAB} is High, the outputs are in the high-impedance state. The High clock can be controlled with the clock-enable inputs ($\overline{CEBA}/\overline{CEAB}$).

Data flow for B-to-A is similar to that of A-to-B but uses \overline{OEBA} , LEBA and \overline{CPBA} .

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}$	TYPICAL		UNIT
			2.5V	3.3V	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	$C_L = 50\text{pF}$	1.9 2.5	1.6 1.9	ns
C_{IN}	Input capacitance DIR, \overline{OE}	$V_I = 0\text{V}$ or V_{CC}	4	4	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; $V_{I/O} = 0\text{V}$ or V_{CC}	8	8	pF
I_{CCZ}	Total supply current	Outputs disabled	40	70	μA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	-40°C to $+85^{\circ}\text{C}$	74ALVT16600 DL	AV16600 DL	SOT371-1
56-Pin Plastic TSSOP Type II	-40°C to $+85^{\circ}\text{C}$	74ALVT16600 DGG	AV16600 DGG	SOT364-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 27	$\overline{OEAB}/\overline{OEBA}$	A-to-B Output enable input (active Low)
29, 56	$\overline{CEBA}/\overline{CEAB}$	B-to-A / A-to-B clock enable (active Low)
2, 28	LEAB/LEBA	A-to-B/B-to-A Latch enable input
55,30	$\overline{CPAB}/\overline{CPBA}$	A-to-B/B-to-A Clock input (active falling edge)
3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	A0-A17	Data inputs/outputs (A side)
54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	B0-B17	Data inputs/outputs (B side)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

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FUNCTION TABLE

INPUTS					OUTPUT
CEAB	OEAB	LEAB	CPAB	A	B
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B _O [±]
L	L	L	↓	L	L
L	L	L	↓	H	H
L	L	L	H	X	B _O [±]
L	L	L	L	X	B _O [§]

X =Don't care

H =High voltage level

L =Low voltage level

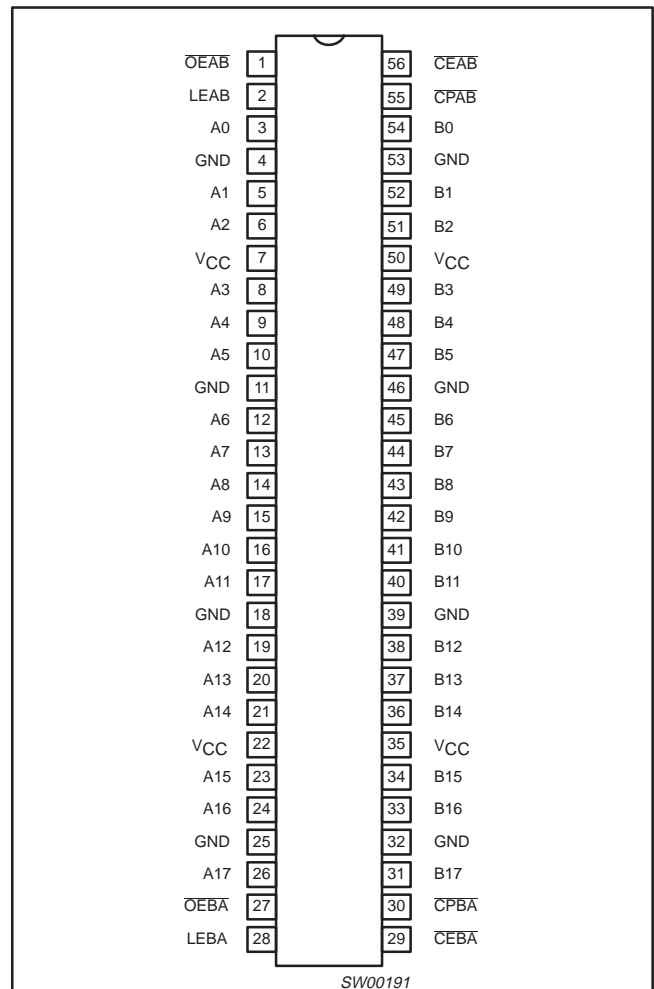
↓ =High-to-Low clock transition

† A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, CPBA, and CEBA.

± Output level before the indicated steady-state input conditions were established.

§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was Low before LEAB went Low.

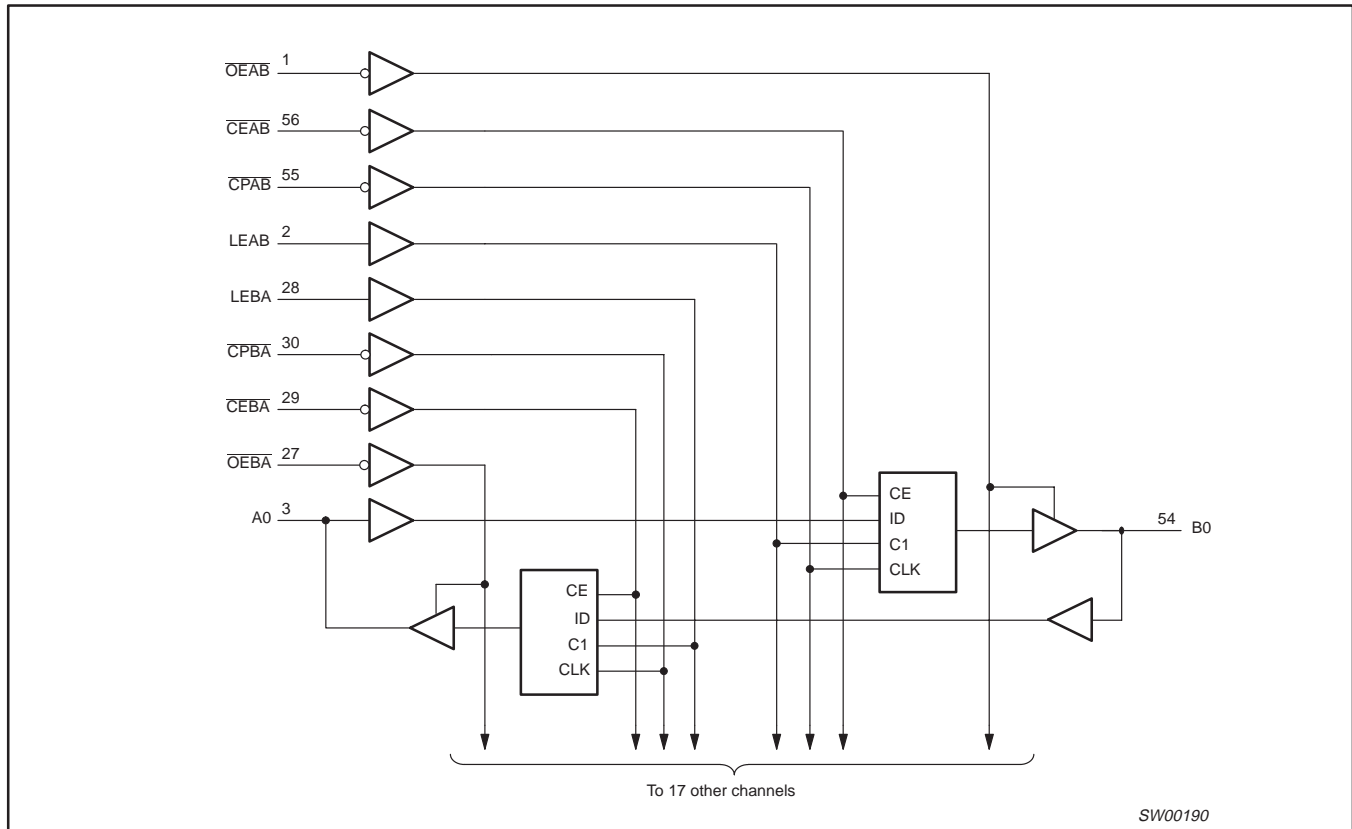
PIN CONFIGURATION



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LOGIC DIAGRAM (Positive Logic)



ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		-0.5 to +4.6	V
I _{IK}	DC input diode current	V _I < 0	-50	mA
V _I	DC input voltage ³		-0.5 to +7.0	V
I _{OK}	DC output diode current	V _O < 0	-50	mA
V _{OUT}	DC output voltage ³	Output in Off or High state	-0.5 to +7.0	V
I _{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T _{stg}	Storage temperature range		-65 to +150	°C

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V _I	Input voltage	0	5.5	0	5.5	V
V _{IH}	High-level input voltage	1.7		2.0		V
V _{IL}	Input voltage		0.7		0.8	V
I _{OH}	High-level output current		-8		-32	mA
I _{OL}	Low-level output current		8		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1 kHz		24		64	
Δt/Δv	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T _{amb}	Operating free-air temperature range	-40	+85	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS (3.3V ± 0.3V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP ¹	MAX	
V _{IK}	Input clamp voltage	V _{CC} = 3.0V; I _{IK} = -18mA		-0.85	-1.2	V
V _{OH}	High-level output voltage	V _{CC} = 3.0 to 3.6V; I _{OH} = -100μA	V _{CC} -0.2	V _{CC}		V
		V _{CC} = 3.0V; I _{OH} = -32mA	2.0	2.3		
V _{OL}	Low-level output voltage	V _{CC} = 3.0V; I _{OL} = 100μA		0.07	0.2	V
		V _{CC} = 3.0V; I _{OL} = 16mA		0.25	0.4	
		V _{CC} = 3.0V; I _{OL} = 32mA		0.3	0.5	
		V _{CC} = 3.0V; I _{OL} = 64mA		0.4	0.55	
V _{RST}	Power-up output low voltage ⁶	V _{CC} = 3.6V; I _O = 1mA; V _I = V _{CC} or GND			0.55	V
I _I	Input leakage current	V _{CC} = 3.6V; V _I = V _{CC} or GND	Control pins	0.1	±1	μA
		V _{CC} = 0 or 3.6V; V _I = 5.5V		0.1	10	
		V _{CC} = 3.6V; V _I = 5.5V	Data pins ⁴	0.1	20	
		V _{CC} = 3.6V; V _I = V _{CC}		0.5	10	
		V _{CC} = 3.6V; V _I = 0V		0.1	-5	
I _{OFF}	Off current	V _{CC} = 0V; V _I or V _O = 0 to 4.5V		0.1	±100	μA
I _{HOLD}	Bus Hold current Data inputs ⁷	V _{CC} = 3V; V _I = 0.8V		75	130	μA
		V _{CC} = 3V; V _I = 2.0V		-75	-140	
		V _{CC} = 0V to 3.6V; V _{CC} = 3.6V		±500		
I _{EX}	Current into an output in the High state when V _O > V _{CC}	V _O = 5.5V; V _{CC} = 3.0V		10	125	μA
I _{PU/PD}	Power up/down 3-State output current ³	V _{CC} ≤ 1.2V; V _O = 0.5V to V _{CC} ; V _I = GND or V _{CC} OE = Don't care		1.0	±100	μA
I _{CCH}	Quiescent supply current	V _{CC} = 3.6V; Outputs High, V _I = GND or V _{CC} , I _O = 0		0.06	0.1	mA
I _{CCL}		V _{CC} = 3.6V; Outputs Low, V _I = GND or V _{CC} , I _O = 0		4.0	5	
I _{CCZ}		V _{CC} = 3.6V; Outputs Disabled; V _I = GND or V _{CC} , I _O = 0 ⁵		0.06	0.1	
ΔI _{CC}	Additional supply current per input pin ²	V _{CC} = 3V to 3.6V; One input at V _{CC} -0.6V, Other inputs at V _{CC} or GND		0.04	0.4	mA

NOTES:

- All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
- This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
- This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100μsec is permitted. This parameter is valid for T_{amb} = 25°C only.
- Unused pins at V_{CC} or GND.
- I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
- This is the bus hold overdrive current required to force the input to the opposite logic state.

2.5V/3.3V 18-bit universal bus transceiver (3-State)

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AC CHARACTERISTICS (3.3V ± 0.3V RANGE)GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 500\Omega$; $T_{\text{amb}} = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$V_{CC} = 3.3V \pm 0.3V$			
			MIN	TYP ¹	MAX	
f_{MAX}	Maximum clock frequency	1		300		MHz
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	2	1.0 1.0	1.6 1.9	2.3 2.8	ns
t_{PLH} t_{PHL}	Propagation delay Clock Low or High LEAB to Bn or LEBA to An	3	1.5 1.5	2.2 2.5	3.3 4.2	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{\text{CPAB}}$ to Bn or $\overline{\text{CPBA}}$ to An	1	1.5 1.5	2.6 3.2	4.2 4.8	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	5 6	1.5 1.0	2.2 1.6	3.4 2.6	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	5 6	1.5 1.5	2.6 2.3	3.8 3.5	ns

NOTE:1. All typical values are at $V_{CC} = 3.3V$ and $T_{\text{amb}} = 25^\circ\text{C}$.**AC SETUP REQUIREMENTS (3.3V ± 0.3V RANGE)**GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 500\Omega$; $T_{\text{amb}} = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			$V_{CC} = 3.3V \pm 0.3V$		
			MIN	TYP ¹	
$t_{\text{s(H)}}$ $t_{\text{s(L)}}$	Setup time, High or Low An to $\overline{\text{CPAB}}$ or Bn to $\overline{\text{CPBA}}$	4	2.0 2.0	0.8 0.9	ns
$t_{\text{h(H)}}$ $t_{\text{h(L)}}$	Hold time, High or Low An to $\overline{\text{CPAB}}$ or Bn to $\overline{\text{CPBA}}$	4	0.0 0.0	-0.9 -0.7	ns
$t_{\text{s(H)}}$ $t_{\text{s(L)}}$	Setup time, High or Low Clock Low An to LEAB or Bn to $\overline{\text{CPBA}}$	4	1.0 1.0	-0.4 -0.1	ns
$t_{\text{h(H)}}$ $t_{\text{h(L)}}$	Hold time, High or Low Clock High An to LEAB or Bn to LEBA	4	1.0 1.0	0.1 0.4	ns
$t_{\text{s(H)}}$ $t_{\text{s(L)}}$	Setup time $\overline{\text{CEAB}}$ before $\overline{\text{CPAB}}$ or $\overline{\text{CEBA}}$ before $\overline{\text{CPBA}}$	4	1.5 1.0	0.3 -0.6	ns
$t_{\text{h(H)}}$ $t_{\text{h(L)}}$	Hold time $\overline{\text{CEAB}}$ after $\overline{\text{CPAB}}$ or $\overline{\text{CEBA}}$ after $\overline{\text{CPBA}}$	4	1.5 1.0	0.7 -0.2	ns
$t_{\text{w(H)}}$ $t_{\text{w(L)}}$	Pulse width, High or Low $\overline{\text{CPAB}}$ or $\overline{\text{CPBA}}$	1	1.5 1.5		ns
$t_{\text{w(H)}}$	LEAB or LEBA pulse width, High	3	1.5		ns

NOTE:1. All typical values are at $V_{CC} = 3.3V$ and $T_{\text{amb}} = 25^\circ\text{C}$.

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DC ELECTRICAL CHARACTERISTICS (2.5V ± 0.2V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP ¹	MAX	
V _{IK}	Input clamp voltage	V _{CC} = 2.3V; I _{IK} = -18mA		-0.85	-1.2	V
V _{OH}	High-level output voltage	V _{CC} = 2.3 to 3.6V; I _{OH} = -100μA	V _{CC} -0.2			V
		V _{CC} = 2.3V; I _{OH} = -8mA	1.8			
V _{OL}	Low-level output voltage	V _{CC} = 2.3V; I _{OL} = 100μA		0.07	0.2	V
		V _{CC} = 2.3V; I _{OL} = 24mA		0.3	0.5	
		V _{CC} = 2.3V; I _{OL} = 8mA			0.4	
V _{RST}	Power-up output low voltage ⁷	V _{CC} = 2.7V; I _O = 1mA; V _I = V _{CC} or GND			0.55	V
I _I	Input leakage current	V _{CC} = 2.7V; V _I = V _{CC} or GND	Control pins	0.1	±1	μA
		V _{CC} = 0 or 2.7V; V _I = 5.5V		0.1	10	
		V _{CC} = 2.7V; V _I = 5.5V		0.1	20	
		V _{CC} = 2.7V; V _I = V _{CC}	Data pins ⁴	0.1	1	
		V _{CC} = 2.7V; V _I = 0		0.1	-5	
I _{OFF}	Off current	V _{CC} = 0V; V _I or V _O = 0 to 4.5V		0.1	±100	μA
I _{HOLD}	Bus Hold current	V _{CC} = 2.3V; V _I = 0.7V		90		μA
	Data inputs ⁶	V _{CC} = 2.3V; V _I = 1.7V		-75		
I _{EX}	Current into an output in the High state when V _O > V _{CC}	V _O = 5.5V; V _{CC} = 2.3V		10	125	μA
I _{PU/PD}	Power up/down 3-State output current ³	V _{CC} ≤ 1.2V; V _O = 0.5V to V _{CC} ; V _I = GND or V _{CC} ; OE = Don't care		1	100	μA
I _{CCH}	Quiescent supply current	V _{CC} = 2.7V; Outputs High, V _I = GND or V _{CC} , I _O = 0		0.04	0.1	mA
I _{CCL}		V _{CC} = 2.7V; Outputs Low, V _I = GND or V _{CC} , I _O = 0		3.0	4.5	
I _{CCZ}		V _{CC} = 2.7V; Outputs Disabled; V _I = GND or V _{CC} , I _O = 0 ⁵		0.04	0.1	
ΔI _{CC}	Additional supply current per input pin ²	V _{CC} = 2.3V to 2.7V; One input at V _{CC} -0.6V, Other inputs at V _{CC} or GND		0.01	0.4	mA

NOTES:

- All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.
- This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.
- This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 2.5V ± 0.2V a transition time of 100μsec is permitted. This parameter is valid for T_{amb} = 25°C only.
- Unused pins at V_{CC} or GND.
- I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
- Not guaranteed.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

2.5V/3.3V 18-bit universal bus transceiver (3-State)

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AC CHARACTERISTICS (2.5V ± 0.2V RANGE)GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 500\Omega$; $T_{\text{amb}} = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$V_{CC} = 2.5V \pm 0.2V$			
			MIN	TYP ¹	MAX	
f_{MAX}	Maximum clock frequency	1		250		MHz
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	2	1.0 1.5	1.9 2.5	3.0 3.6	ns
t_{PLH} t_{PHL}	Propagation delay Clock Low or High LEAB to Bn or LEBA to An	3	2.0 2.5	3.0 3.3	4.5 5.1	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{\text{CPAB}}$ to Bn or $\overline{\text{CPBA}}$ to An	1	2.5 2.5	3.8 4.5	5.6 6.7	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	5 6	2.0 1.0	3.1 2.0	4.4 3.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	5 6	1.5 1.5	2.5 2.3	4.1 3.6	ns

NOTE:1. All typical values are at $V_{CC} = 3.3V$ and $T_{\text{amb}} = 25^\circ\text{C}$.**AC SETUP REQUIREMENTS (2.5V ± 0.2V RANGE)**GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 500\Omega$; $T_{\text{amb}} = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			$V_{CC} = 2.5V \pm 0.2V$		
			MIN	TYP ¹	
$t_{\text{s(H)}}$ $t_{\text{s(L)}}$	Setup time, High or Low An to $\overline{\text{CPAB}}$ or Bn to $\overline{\text{CPBA}}$	4	1.5 2.0	0.5 1.1	ns
$t_{\text{h(H)}}$ $t_{\text{h(L)}}$	Hold time, High or Low An to $\overline{\text{CPAB}}$ or Bn to $\overline{\text{CPBA}}$	4	0.0 1.0	-1.1 -0.4	ns
$t_{\text{s(H)}}$ $t_{\text{s(L)}}$	Setup time, High or Low Clock Low An to LEAB or Bn to $\overline{\text{CPBA}}$	4	0.0 1.5	-0.8 0.4	ns
$t_{\text{h(H)}}$ $t_{\text{h(L)}}$	Hold time, High or Low Clock High An to LEAB or Bn to LEBA	4	1.0 1.5	-0.4 0.9	ns
$t_{\text{s(H)}}$ $t_{\text{s(L)}}$	Setup time $\overline{\text{CEAB}}$ before $\overline{\text{CPAB}}$ or $\overline{\text{CEBA}}$ before $\overline{\text{CPBA}}$	4	1.0 1.0	-0.3 -0.5	ns
$t_{\text{h(H)}}$ $t_{\text{h(L)}}$	Hold time $\overline{\text{CEAB}}$ after $\overline{\text{CPAB}}$ or $\overline{\text{CEBA}}$ after $\overline{\text{CPBA}}$	4	1.5 1.5	0.8 0.5	ns
$t_{\text{w(H)}}$ $t_{\text{w(L)}}$	Pulse width, High or Low $\overline{\text{CPAB}}$ or $\overline{\text{CPBA}}$	1	2.5 2.5		ns
$t_{\text{w(H)}}$	LEAB or LEBA pulse width, High	3	1.5		ns

NOTE:1. All typical values are at $V_{CC} = 2.5V$ and $T_{\text{amb}} = 25^\circ\text{C}$.

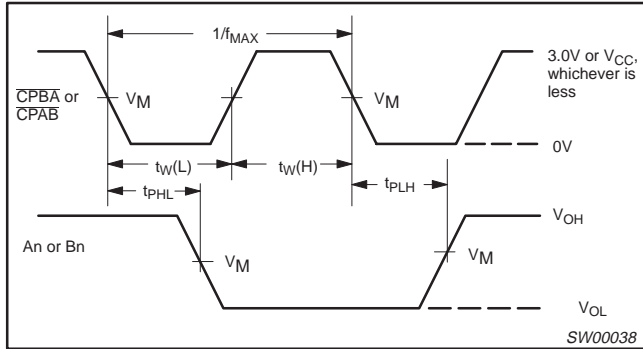
2.5V/3.3V 18-bit universal bus transceiver (3-State)

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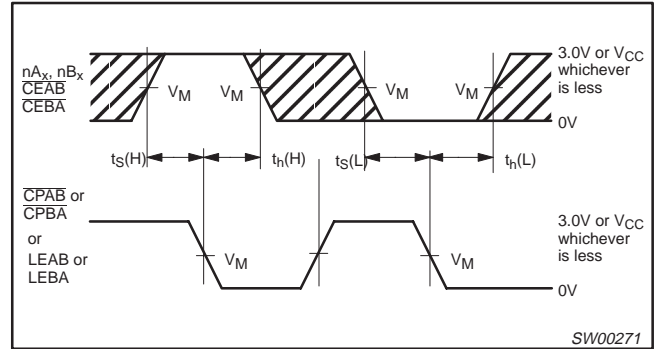
AC WAVEFORMS

NOTES:

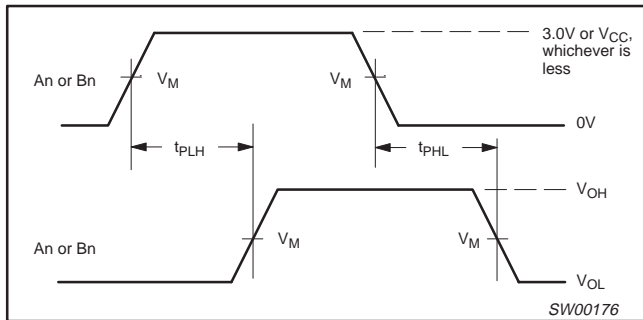
1. $V_M = 1.5V$ at $V_{CC} \geq 3.0V$, $V_M = V_{CC}/2$ at $V_{CC} \leq 2.7V$
2. $V_X = V_{OL} + 0.3V$ at $V_{CC} \geq 3.0V$, $V_X = V_{OL} + 0.15V$ at $V_{CC} \leq 2.7V$
3. $V_Y = V_{OH} - 0.3V$ at $V_{CC} \geq 3.0V$, $V_Y = V_{OH} - 0.15V$ at $V_{CC} \leq 2.7V$



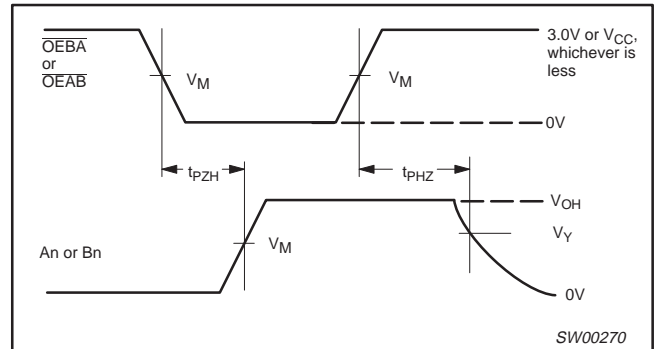
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



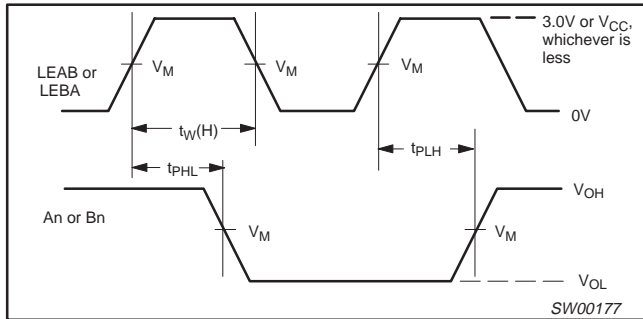
Waveform 4. Data Setup and Hold Times



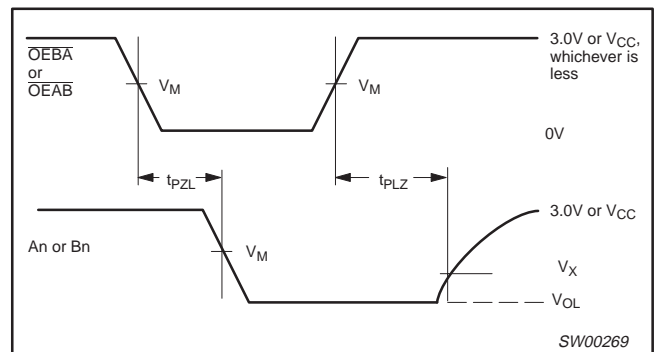
Waveform 2. Propagation Delay, Transparent Mode



Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 3. Propagation Delay, Enable to Output, and Enable Pulse Width



Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

2.5V/3.3V 18-bit universal bus transceiver (3-State)

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TEST CIRCUIT AND WAVEFORMS

Test Circuit for 3-State Outputs

The test circuit shows a Pulse Generator connected to the input of a D.U.T. (Device Under Test) through a termination resistor R_T . The output of the D.U.T. is connected to a load resistor R_L and a load capacitor C_L . A switch selects between a 6.0V or $V_{CC} \times 2$ source and a GND source for the load resistor. The output voltage is labeled V_{OUT} .

SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6V or $V_{CC} \times 2$
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

INPUT PULSE REQUIREMENTS

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ALVT16	3.0V or V_{CC} whichever is less	$\leq 10\text{MHz}$	500ns	$\leq 2.5\text{ns}$	$\leq 2.5\text{ns}$

The waveforms show a negative pulse and a positive pulse. The negative pulse starts at 90% V_{IN} and falls to 10% V_{IN} (labeled V_M) with a fall time $t_{THL} (t_F)$. It remains at 10% V_{IN} for a pulse width t_W before rising back to 90% V_{IN} with a rise time $t_{TLH} (t_R)$. The positive pulse starts at 10% V_{IN} and rises to 90% V_{IN} (labeled V_M) with a rise time $t_{TLH} (t_R)$. It remains at 90% V_{IN} for a pulse width t_W before falling back to 10% V_{IN} with a fall time $t_{THL} (t_F)$.

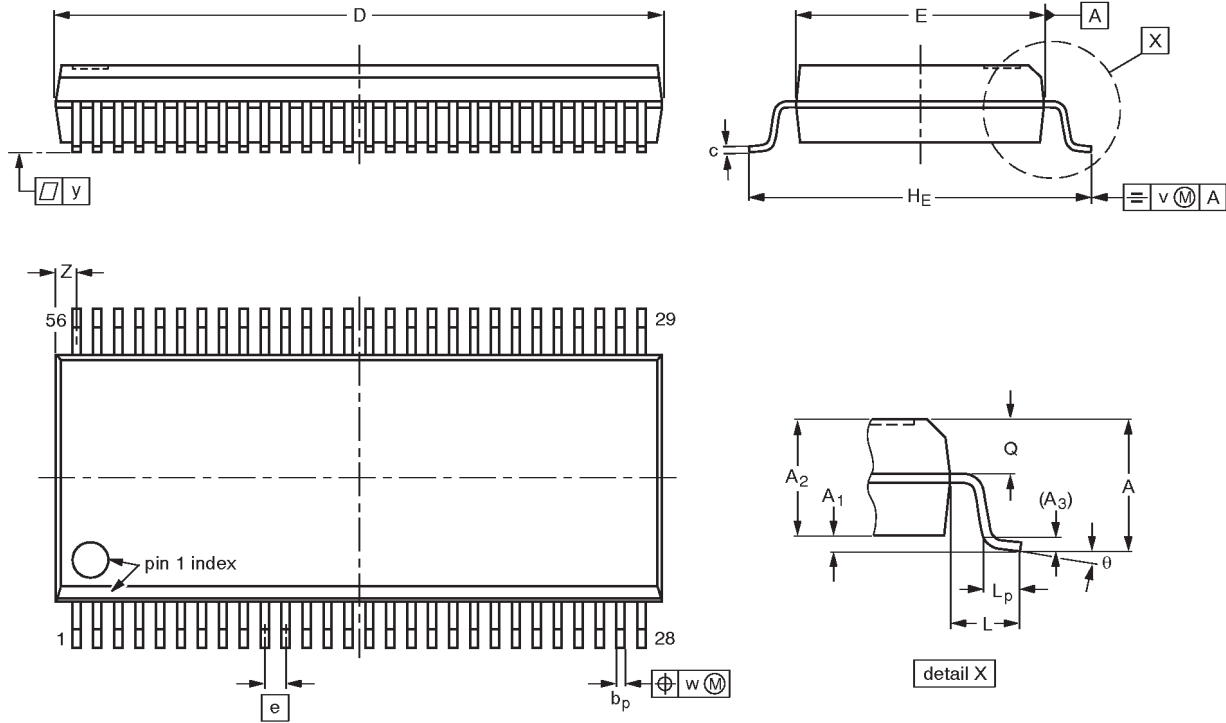
SW00025

2.5V/3.3V 18-bit universal bus transceiver (3-State)

74ALVT16600

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm

SOT371-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	18.55 18.30	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

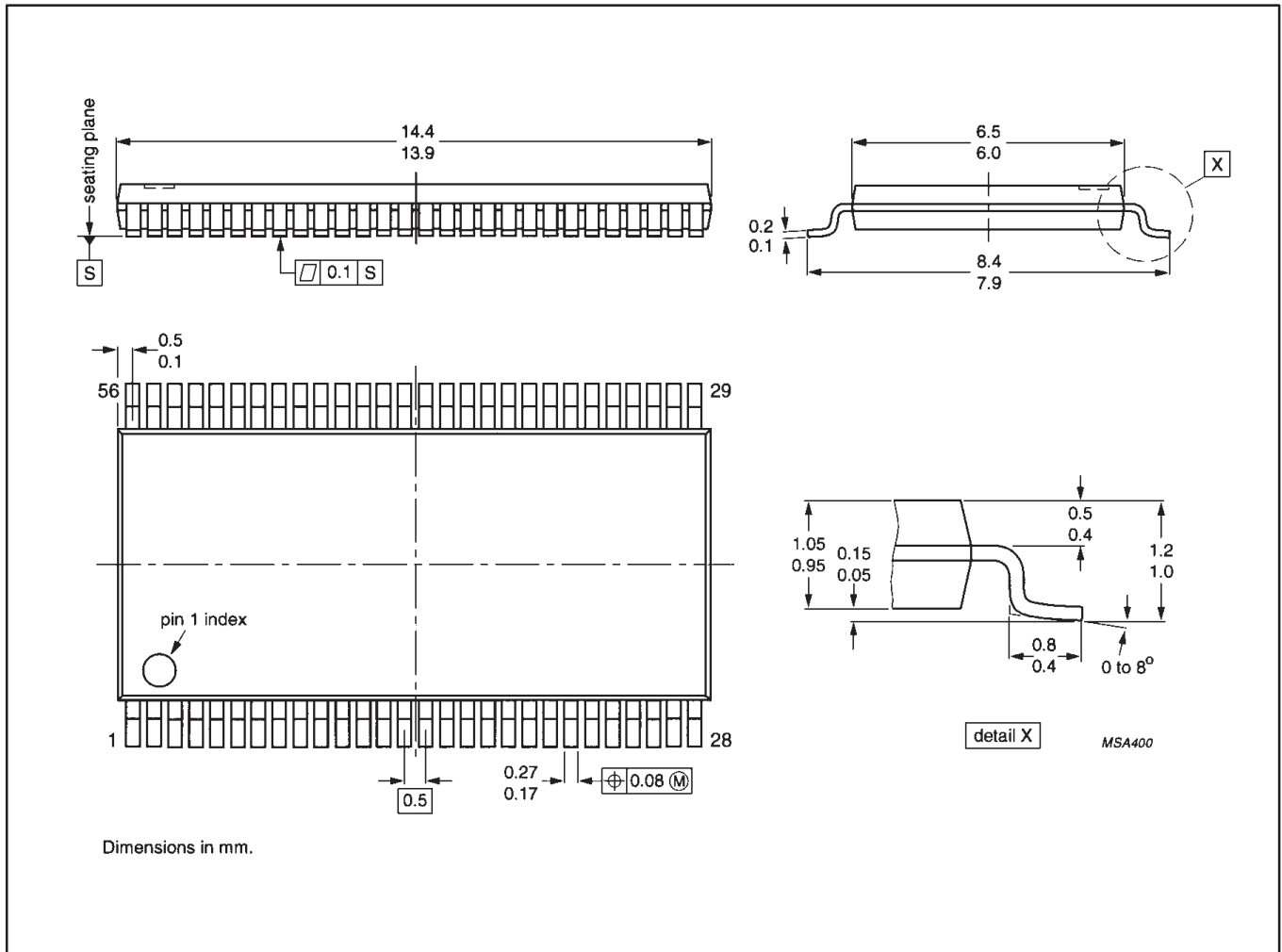
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT371-1		MO-118AB				93-11-02 95-02-04

2.5V/3.3V 18-bit universal bus transceiver (3-State)

74ALVT16600

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm

SOT364-1



2.5V/3.3V 18-bit universal bus transceiver (3-State)

74ALVT16600

NOTES

2.5V/3.3V 18-bit universal bus transceiver (3-State)

74ALVT16600

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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